

**Notice of References Cited**

Application/Control No.

10/644,730

Applicant(s)/Patent Under  
Reexamination  
SEKIDO ET AL.

Examiner

Andre Pierre-Louis

Art Unit

2123

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,795,802	09-2004	Yonezawa et al.	703/19
*	B	US-2003/0228714	12-2003	Smith et al.	438/8
*	C	US-2004/0040000	02-2004	Taravade et al.	716/4
*	D	US-6,144,931	11-2000	Toda, Takeshi	703/13
*	F	US-2003/0237064	12-2003	White et al.	716/5
*	F	US-2002/0152447	10-2002	Venugopal et al.	716/4
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Krabbenborg et al. (IEEE 1996) teaches a Layout to Circuit Extraction for Three-Dimension Thermal-Electrical Circuit Simulation of Device Structures, Pgs.765-774.
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.